W83L784R/W83L784G
Winbond H/W
Monitoring IC

Publication Release Date: Jan. 2005

W83L784R
Data Sheet Revision History

	PAGES	DATES	VERSION	VERSION ON WEB	MAIN CONTENTS
1	n.a.			n.a.	All the versions before 0.50 are for internal use.
2	n.a.	4/99	0.5	n.a.	First publication.
3	P.56-57	6/99	0.52	n.a.	Schematics updated
4	P.56	6/99	0.53	n.a.	Corrected the length (D) from 10.2mm to 7.2mm in the package outline table.
5	P.57	9/99	0.54	n.a.	Updated V0.5 schematics adding pull-high resistors for RESET# (pin15)
6	P.36 P. 9	10/99	0.55	n.a.	This update is for **C version** IC. Update CR [54h] register for PWMOUT function. Change Pin 15 from output to open-drain.
7	n.a.	4/02	1.0	1.0	Change version and version on web site to 1.0
8	n.a.	4/06	1.1	1.1	Add lead-free package version

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1. GENERAL DESCRIPTION

W83L784R/G is an evolving product of W83782D/G --- Winbond's most popular hardware status monitoring IC. Specifically designed for the Notebook system, W83L784R/G can be used to monitor several critical hardware parameters of the system, including power supply voltages, fan speeds, and temperatures, which are very important for a high-end Notebook system to work stably and properly.

An 8-bit analog-to-digital converter (ADC) is built inside W83L784R/G. The W83L784R/G can monitor 4 analog voltage inputs, 2 fan tachometer inputs, one on-chip internal temperature sensor and 2 remote temperature sensors. The remote temperature sensing can be performed by thermistors, or 2N3904 NPN-type transistors, or directly from Intel™ Deschutes CPU thermal diode output. The W83L784R/G provides 2 PWM (pulse width modulation) outputs for the fan speed control to support the **"** Thermal Cruise™ **"** system, which can maintain the CPU or system in the specific programmable temperature under the hardware control. Another Fan speed control mode is **"**Speed Cruise**"** to keep the fan operating in the specific RPM. On the other hand, the W83L784R/G provides low active outputs such as fan fault and Battery low which could issue the hardware warning signals when the fan speed or battery voltage drop out of the preset range. Also the W83L784R/G provides power good reset for 3V and 5V; power down mode for power saving; fault pin for necessary H/W shutdown control; SMI#, OVT#, GPO# signals for system protection events; I^2C™ serial bus interface.

Through the application software or BIOS, the users can read all the monitored parameters of system from time to time. And a pop-up warning can be also activated when the monitored item was out of the proper/preset range. The application software could be Winbond's Hardware Doctor™, or Intel™ LDCM (LanDesk Client Management), or other management application software. Also the users can set up the upper and lower limits (alarm thresholds) of these monitored parameters and to activate one programmable and maskable interrupts. For the spacing saving consideration of the Notebook system, W83L784R/G is in the package of 209mil 20pins-SSOP.

2. FEATURES

2.1 Monitoring Items

- 2 thermal inputs from remote thermistors or 2N3904 NPN-type transistors or Pentium™ II (Deschutes) thermal diode output
- One on-chip temperature detection
- 4 voltage inputs
  --- typical for Vcore, +3.3V, +5V, Battery
- 2 sets of fan speed control and fan speed monitoring input
- WATCHDOG comparison of all monitored values
- Programmable hysteresis and setting points (alarm thresholds) for all monitored items

2.2 Actions Enabling

- Issue fan fault signal as fans are abnomally stopped
- Issue battery low signal as bettery voltage is abnomally out of range
- 2 PWM (pulse width modulation) outputs for fan speed control to support " Thermal Cruise™ " or " Speed Cruise™ "

--- Automatically maintain the CPU or system in the specific temperature or keep the fans in the specific speed under the H/W control

- Issue SMI#, OVT#, GPO to activate system protection
- PWR_DN# setting for the Power down mode
- Warning signal pop-up in application software

2.3 Power Good

- Issue RESET# outputs as the Power Good signal when 3V and 5V rise across a reset threshold.

2.4 General

- I^2C™ serial bus interface
- Intel™ LDCM (DMI driver 2.0) support
- Acer™ ADM (DMI driver 2.0) support
- Winbond hardware monitoring application software (Hardware Doctor™) support, for both Windows 95/98
- Meet WfM 2.0 (Wired for Management) spec.
- 5V Vcc operation

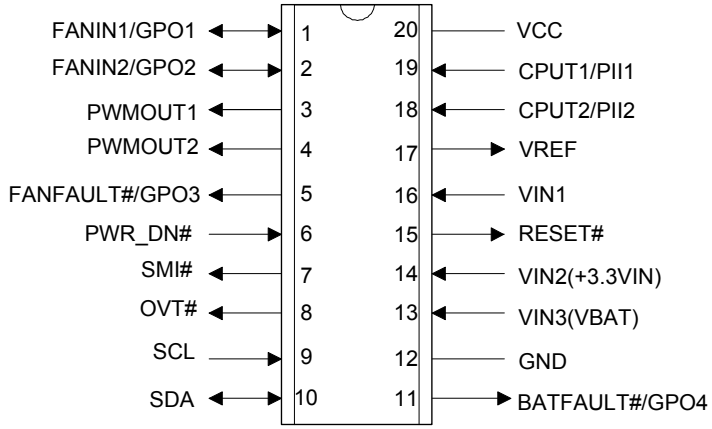
2.5 Package

- 20-pin SSOP (209mil)

3. KEY SPECIFICATIONS

• Voltage monitoring accuracy		±1% (Max)
• Monitoring Temperature Range and Accuracy	- 40°C to +120°C	± 3°C(Max)
• Supply Voltage		5V
• Operating Supply Current		2 mA typ.
• Power Down Suppy Current		0.5 mA typ.
• ADC Resolution		8 Bits

4. PIN CONFIGURATION



5. PIN DESCRIPTION

I/O_{12t} - TTL level bi-directional pin with 12 mA source-sink capability

I/O_{12ts} - TTL level and schmitt trigger

OUT_{12} - Output pin with 12 mA source-sink capability

AOUT - Output pin(Analog)

OD_{12} - Open-drain output pin with 12 mA sink capability

IN_t - TTL level input pin

IN_{ts} - TTL level input pin and schmitt trigger

AIN - Input pin(Analog)

PIN NAME	PIN NO.	TYPE	DESCRIPTION
FANIN1 / GPO1	1	IN_{ts} / OUT_{12}	0V to +5V amplitude fan tachometer input. (Default) / General purpose output. This multi-functional pin is programmable.
FANIN2 / GPO2	2	IN_{ts} / OUT_{12}	0V to +5V amplitude fan tachometer input. (Default) / General purpose output. This multi-functional pin is programmable.
PWMOUT1	3	OD_{12} / OUT_{12}	Fan speed control PWM output. This pin is **default** open-drain. It can be programmed as an output pin which can drive a HIGH or a LOW.
PWMOUT2	4	OD_{12} / OUT_{12}	Fan speed control PWM output. This pin is **default** open-drain. It can be programmed as an output pin which can drive a HIGH or a LOW.
FANFAULT# / GPO3	5	OD_{12}	Active-Low output. This pin will be a logic LOW when fan1 or fan2 is abnormally stopped. (Default) / General purpose output. This multi-functional pin is programmable.
PWR_DN#	6	IN_t	Power down input. When set this pin LOW, all output pins would be tristate except the pin15 RESET# which will keep HIGH.
SMI#	7	OD_{12}	System Management Interrupt.
OVT#	8	OD_{12}	Over temperature Shutdown Output.
SCL	9	IN_{ts}	Serial Bus Clock.
SDA	10	OD_{12}	Serial Bus bi-directional Data.
BATFAULT# / GPO4	11	OD_{12}	Active-Low output. This pin will be a logic LOW when Battery abnormally drops below the low limit or above the high limit. (Default) / General purpose output. This multi-functional pin is programmable.
GND	12	Ground	Ground.
VIN3(VBAT)	13	AIN	0V to 4.096V FSR Analog Inputs. (This pin should be connected to DC BATTERY. If this voltage is above 4.096V, it should be reduced with the external resistors so that the input voltage will be under 4.096V)

PIN DESCRIPTION, continued.

PIN NAME	PIN NO.	TYPE	DESCRIPTION
VIN2(+3.3VIN)	14	AIN	0V to 4.096V FSR Analog Inputs. (This pin should be connected to 3VCC)
RESET#	15	OD_{12}	Active-Low reset output. RESET# remains LOW while the 5VCC and +3.3V are below the reset threshold. It remains LOW for 200ms after the reset condition is terminated.
VIN1(VCORE)	16	AIN	0V to 4.096V FSR Analog Inputs.
VREF	17	AOUT	Reference Voltage.
CPUT2 / PII2	18	AIN	Thermistor terminal input.(Default) / Pentium™ II diode input. This multi-functional pin is programmable.
CPUT1 / PII1	19	AIN	Thermistor terminal input.(Default) / Pentium™ II diode input. This multi-functional pin is programmable.
VCC	20	POWER	+5VCC power supply input.

6. FUNCTIONAL DESCRIPTION

6.1 General Description

The W83L784R/G provides at most 4 analog positive inputs, 2 fan speed monitors, 2 sets for fan PWM (Pulse Width Modulation) Smart Fan Control , 2 remote thermal inputs from remote thermistors or 2N3904 transistors or Pentium™ II (Deschutes) thermal diode outputs and one on-chip thermal detection. W83L784R/G also provides the power good (reset) output for 3V and 5V power detection and two fault output pins issuing hardware warning if battery and fans become abnormal. When starting the monitor function on the chip, the watch dog machine monitor every function and store the value to registers. If the monitor value exceeds the limit value, the interrupt status will be set to 1.

6.2 Access Interface

The W83L784R/G provides I^2C Serial Bus to read/write internal registers. In the W83L784R/G there are three serial bus addresses. The first address defined at CR [4Ah] can read/write all registers excluding CPUT1/CPUT2 temperature sensor registers and its address default value is 0101101. The address for CPUT1 defined at CR [4Bh] bit2-0 only read/write CPUT1 temperature sensor registers and the address default value is 1001001. The address for CPUT2 defined at CR [4Bh] bit2-0 only read/write CPUT1 temperature sensor registers and the address default value is 1001000.

6.2.1 The first serial bus access timing is shown as follows:

(a) Serial bus write to internal address register followed by the data byte

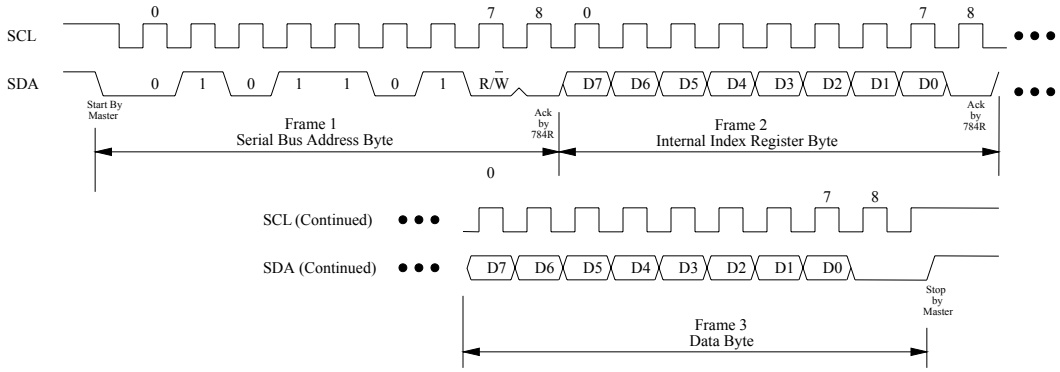


Figure 1. Serial Bus Write to Internal Address Register followed by the Data Byte

(b) Serial bus write to internal address register only

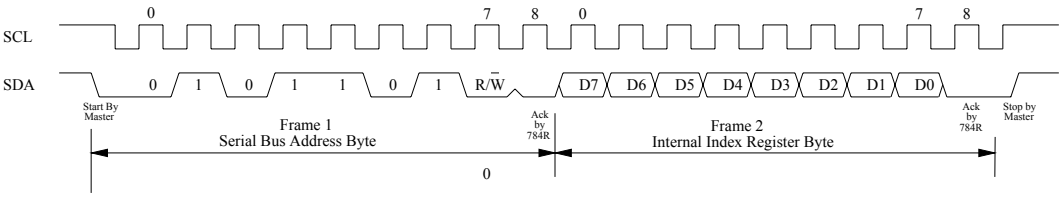


Figure 2. Serial Bus Write to Internal Address Register Only

(c) Serial bus read from a register with the internal address register prefer to desired location

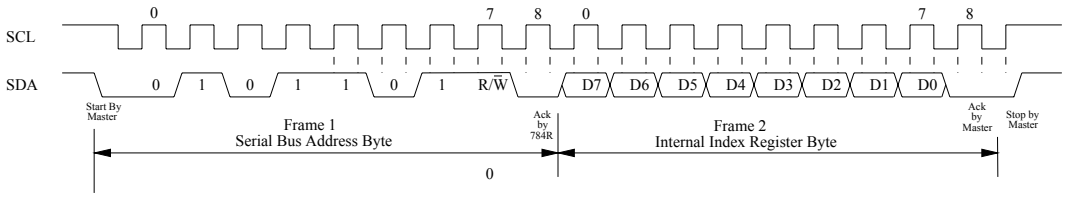


Figure 3. Serial Bus Read from Internal Address Register

6.2.2 The serial bus timing of the temperature CPUT1 and CPUT2 is shown as follow:

(a) Typical 2-byte read from preset pointer location (Temp, T_{OS}, T_{HYST})

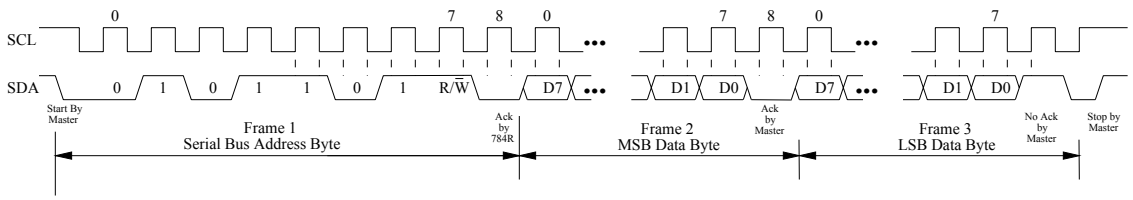


Figure 4. Typical 2-Byte Read From Preset Pointer Location

(b)Typical pointer set followed by immediate read for 2-byte register (Temp, T_{OS}, T_{HYST})

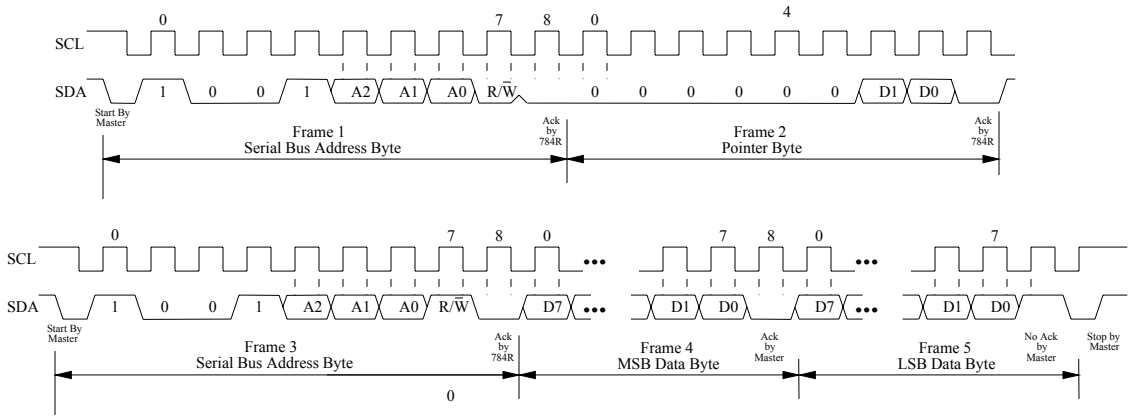


Figure 5. Typical Pointer Set Followed by Immediate Read for 2-Byte Register

(c) Typical read 1-byte from configuration register with preset pointer

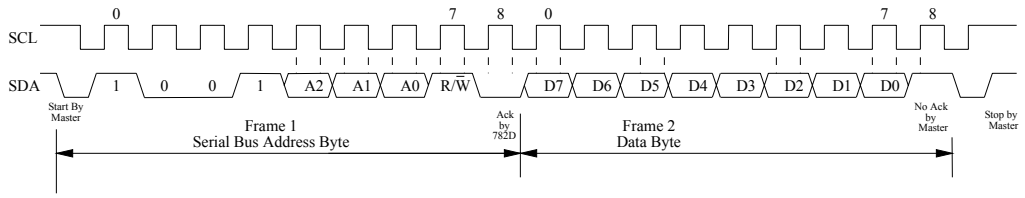


Figure 6. Typical 1-Byte Read From Configuration With Preset Pointer

(d) Typical pointer set followed by immediate read from configuration register

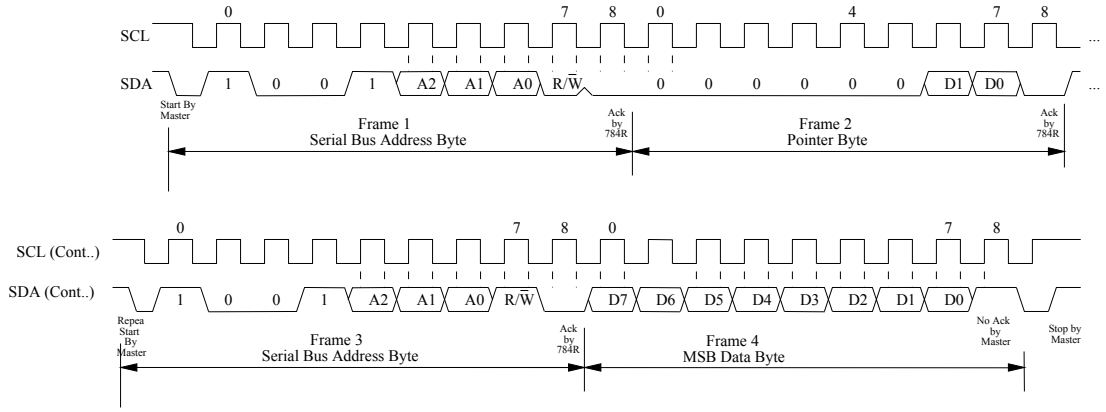


Figure 7. Typical Pointor Set Followed by Immediate Read from Temp 2/3 Configuration Register

(e) Temperature configuration register Write

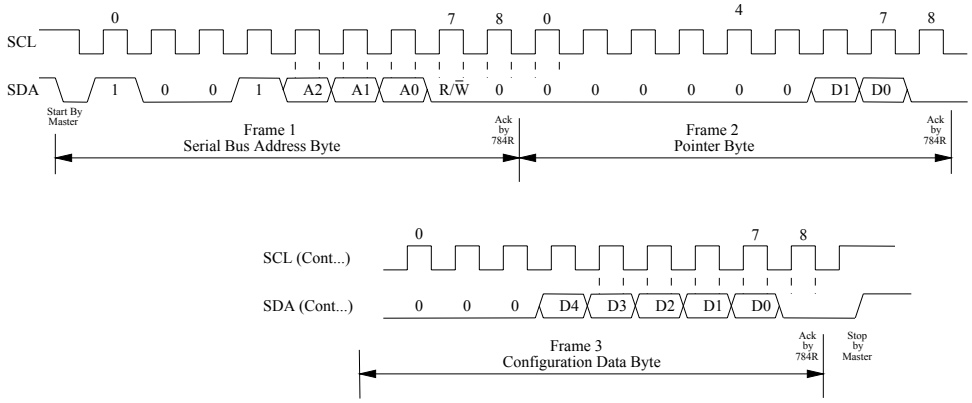


Figure 8. Configuration Register Write

(f) Temperature T_{OS} and T_{HYST} write

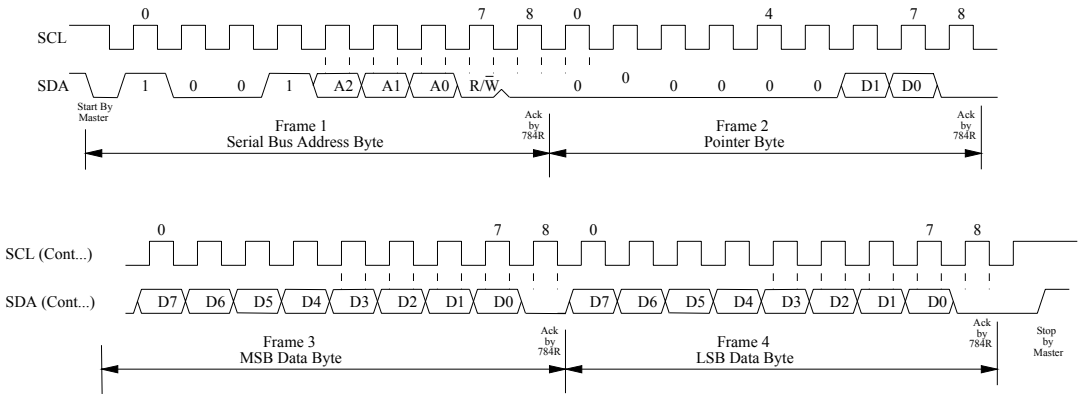


Figure 9. Configuration Register Write

6.3 Analog Inputs

The maximum input voltage of the analog pin is 4.096V because the 8-bit ADC has a 16mv LSB. Really, the application of the PC monitoring would most often be connected to power suppliers. The CPU V-core voltage and +3.3V voltage can directly connected to these analog inputs. The 5VSB and battery inputs should be reduced a factor with external resistors so as to obtain the input range. As Figure 10 shows.

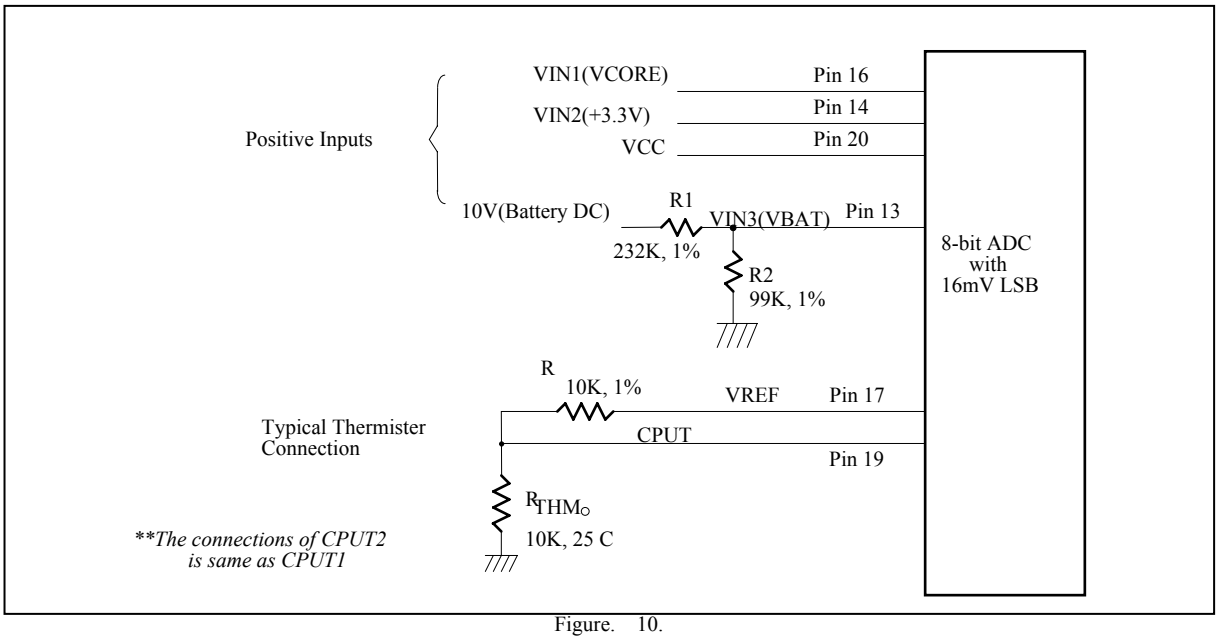


Figure. 10.

6.3.1 Monitor over 4.096V voltage:

The input voltage VIN3 can be expressed as following equation.

$$VIN3 = V_{BAT-DC} \times \frac{R_2}{R_1 + R_2}$$

The value of R1 and R2 can be selected to 232K Ohms and 99K Ohms, respectively, when the input voltage V_{BAT-DC} is 10V. The node voltage of VIN3 can be subject to less than 4.096V for the maximum input range of the 8-bit ADC. The pin 24 is connected to the power supply VCC with +5V. There are two functions in this pin with 5V. The first function is to supply internal analog power in the W83L784R and the second function is that this voltage with 5V is connected to internal serial resistors to monitor the +5V voltage. The values of two serial resistors are 34K ohms and 50K ohms so that input voltage to ADC is 2.98V which is less than 4.096V of ADC maximum input voltage. The express equation can represent as follows.

$$V_{in} = VCC \times \frac{50K\Omega}{50K\Omega + 34K\Omega} \cong 2.98V$$

where VCC is set to 5V

6.3.2 Power good for 3V and 5V

On power up, once VCC (5V) reaches 1V, RESET# will be logic low. As 3V and VCC (5V) rise, RESET# remains asserted. If 3V and VCC (5V) both exceed the reset threshold, RESET becomes logic high after a time equal to the reset pulse width (tRST, typically 200ms). (Figure 11) If a power fail or a brownout happens (i.e. 3V or VCC (5V) drops below the threshold), RESET# output is asserted. As long as the 3V and VCC (5V) remain below the reset threshold, RESET# output remains asserted. Therefore, a brownout condition that interrupts a previously initiated reset pulse causes an additional 200ms delay from the time the latest interruption occurred. On power-on, once 3Vor VCC (5V) drops below the reset threshold, RESET# are guaranteed to be asserted for VCC ≥ 1V.

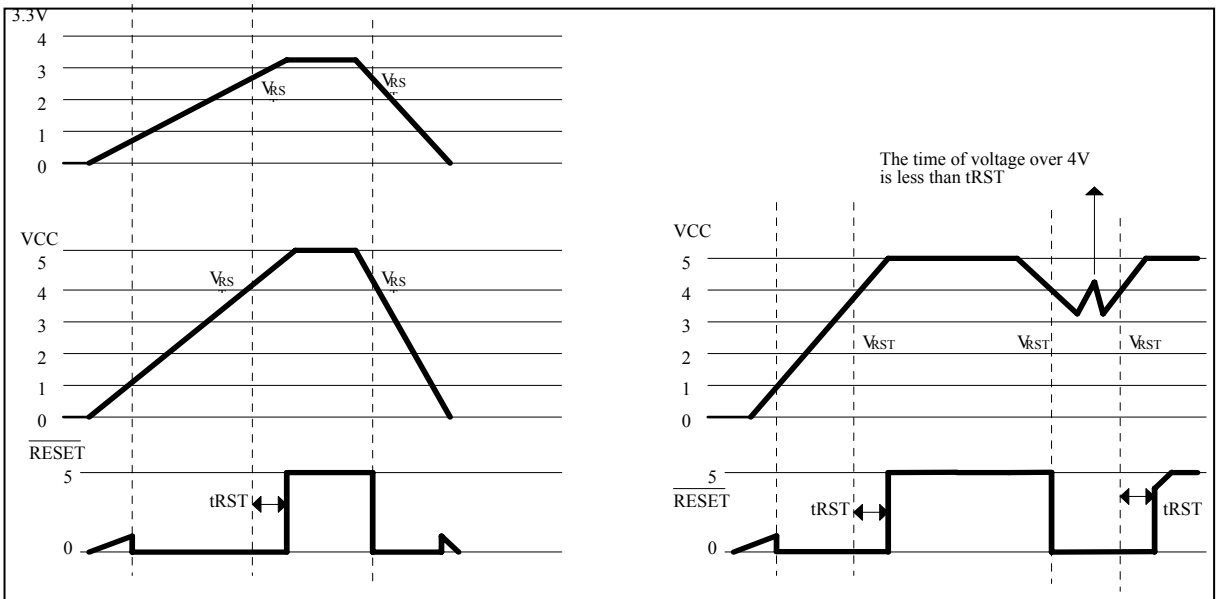


Figure 11

6.3.3 Battery Fault Alarm

W83L784R/G provides a good protection for DC battery. Set VIN3 to monitor DC battery voltage and enable VBAT fault function. When VIN3 (pin13) voltage exceeds high or low limit value, pin BATFAULT# will be asserted.

6.4 Temperature Measurement Machine

The temperature data format is 8-bit two-complement for internal sensor and 9-bit two -complement for sensor CPUT1 and CPUT2. The 8-bit temperature data can be obtained by reading the CR [27h]. The 9-bit temperature data (CPUT1 and CPUT2) can be obtained by reading CR [00h] of its serial bus address. The format of the temperature data is show in Table 1.

Table 1

TEMPERATURE	8-BIT DIGITAL OUTPUT		9-BIT DIGITAL OUTPUT	
	8-BIT BINARY	8-BIT HEX	9-BIT BINARY	9-BIT HEX
+125°C	0111,1101	7Dh	0,1111,1010	0FAh
+25°C	0001,1001	19h	0,0011,0010	032h
+1°C	0000,0001	01h	0,0000,0010	002h
+0.5°C	-	-	0,0000,0001	001h
+0°C	0000,0000	00h	0,0000,0000	000h
-0.5°C	-	-	1,1111,1111	1FFh
-1°C	1111,1111	FFh	1,1111,1110	1FFh
-25°C	1110,0111	E7h	1,1100,1110	1CEh
-55°C	1100,1001	C9h	1,1001,0010	192h

6.4.1 Monitor temperature from thermistor:

The W83L784R/G can connect three thermistors to measure three different envirment temperature. The specification of thermistor should be considered to (1) β value is 3435K, (2) resistor value is 10K ohms at 25°C. In the Figure 10, the themistor is connected by a serial resistor with 10K Ohms, and then connect to VREF (pin 17).

6.4.2 Monitor temperature from Pentium IITM thermal diode or bipolar transistor 2N3904

The W83L784R/G can alternate the thermistor to Pentium II™ (Deschutes) thermal diode interface or transistor 2N3904 and the circuit connection is shown as Figure 12. The pin of Pentium II™ D- is connected to power supply ground (GND) and the pin D+ is connected to pin PIIx in the W83L784R/G. The resistor R=30K ohms should be connected to VREF to supply the diode bias current and the bypass capacitor C=3300pF should be added to filter the high frequency noise. The transistor 2N3904 should be connected to a form with a diode, that is, the Base (B) and Collector (C) in the 2N3904 should be tied together to act as a thermal diode.

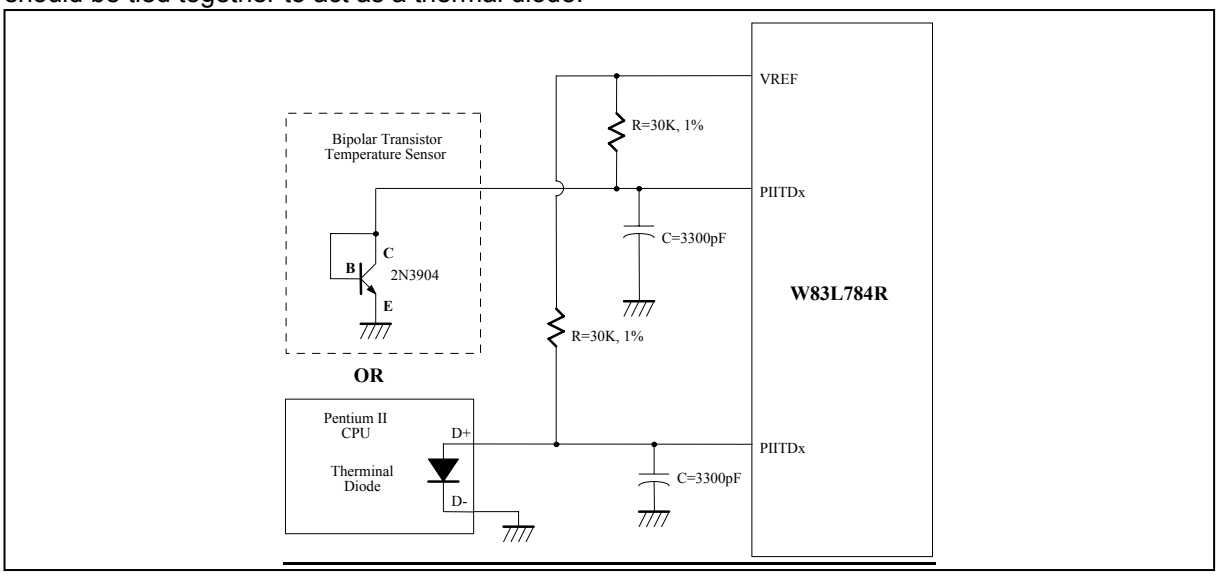


Figure 12

6.4.3 Over Temperature

W83L784R/G provides two external thermal sensors to detect temperature. When detected temperature exceeds the over-temperature value, pin OVT# will be asserted until the temperature goes below the hysteresis temperature. Pin OVT# has 3 operating modes.

6.4.3.1. ACPI Mode

At this mode, temperature exceeding one level of temperature separation, starting from 0 degree, causes the OVT# output activated. OVT# will be activated again once temperature exceeding the next level. OVT# output will act the same manner when temperature goes down. (Figure 13) The

granularity of temperature separation between each OVT# output signal can be programmed at Bank0 CR [4Fh].

The priority of this mode is higher than Comparator mode and Interrupt mode.

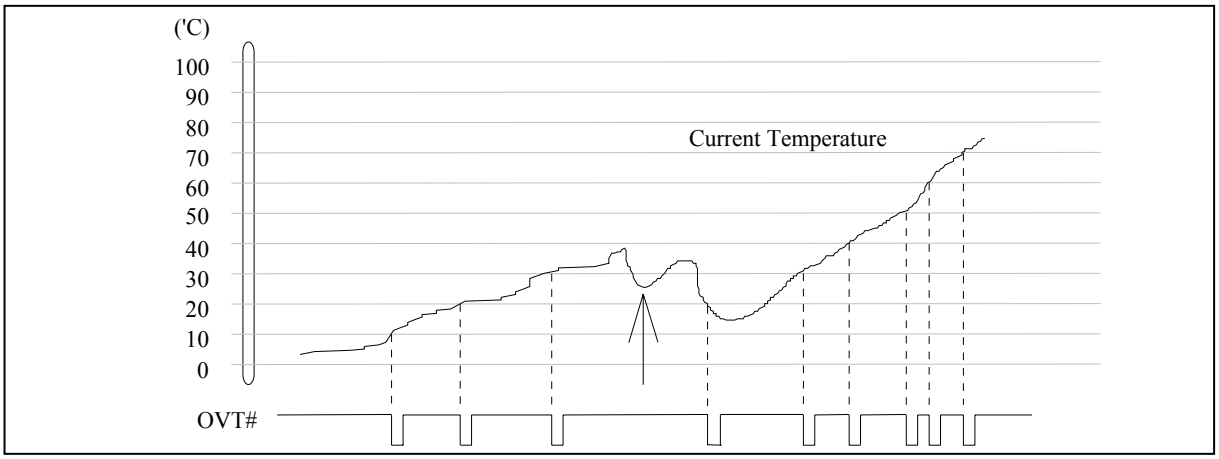


Figure 13

6.4.3.2. Comparator Mode

At this mode, temperature exceeding T_O causes the OVT# output activated until the temperature is less than T_{HYST}. (Figure 14)

6.4.3.3. Interrupt Mode

At this mode, temperature exceeding T_O causes the OVT# output activated indefinitely until reset by reading CPUT1 or CPUT2 registers. Temperature exceeding T_O, then OVT# asserted, and then temperature going below T_{HYST} will also cause the OVT# activated indefinitely until reset by reading temperature sensor2 or sensor 3 registers. Once the OVT# is activated by exceeding T_O, then reset, if the temperature remains above T_{HYST}, the OVT# will not be activated again.(Figure 14)

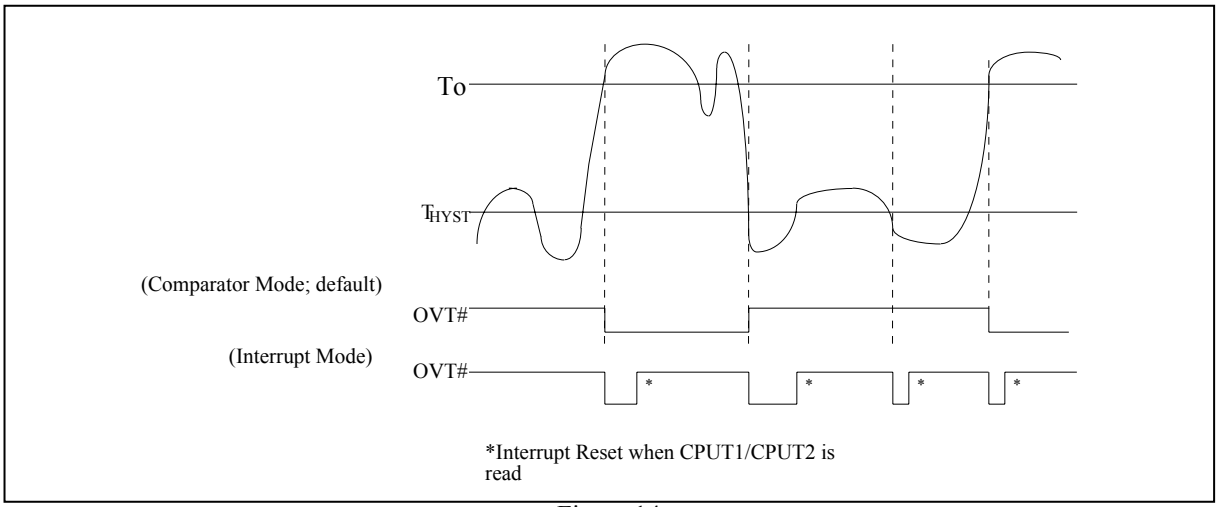


Figure 14

6.5 FAN Speed Count and FAN Speed Control

6.5.1 Fan speed count

Inputs are provides for signals from fans equipped with tachometer outputs. The level of these signals should be set to TTL level, and maximum input voltage can not be over +5.5V. If the input signals from the tachometer outputs are over the VCC, the external trimming circuit should be added to reduce the voltage to obtain the input specification. The normal circuit and trimming circuits are shown as Figure 15.

Determine the fan counter according to:

$$Count = \frac{1.35 \times 10^6}{RPM \times Divisor}$$

In other words, the fan speed counter has been read from register CR28 or CR29 or CR2A, the fan speed can be evaluated by the following equation.

$$RPM = \frac{1.35 \times 10^6}{Count \times Divisor}$$

The default divisor is 2 and defined at CR49.bit0~2, bit4~6 which are three bits for divisor. That provides very low speed fan counter such as power supply fan. The followed table is an example for the relation of divisor, PRM, and count.

Table 2

DIVISOR	NOMINAL PRM	TIME PER REVOLUTION	COUNTS	70% RPM	TIME FOR 70%
1	8800	6.82 ms	*153*	6160	9.74 ms
2 (default)	4400	13.64 ms	*153*	3080	19.48 ms
4	2200	27.27 ms	*153*	1540	38.96 ms
8	1100	54.54 ms	*153*	770	77.92 ms
16	550	109.08 ms	*153*	385	155.84 ms
32	275	218.16 ms	*153*	192	311.68 ms
64	137	436.32 ms	*153*	96	623.36 ms
128	68	872.64 ms	*153*	48	1246.72 ms

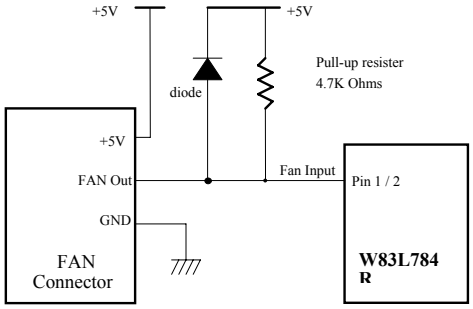


Figure 15-1. Fan with Tach Pull-Up to +5V

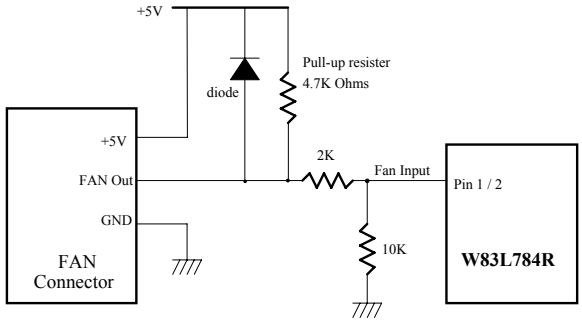


Figure 15-2. Fan with Tach Pull-Up to +5V, or Totem-Pole Output and Register Attenuator

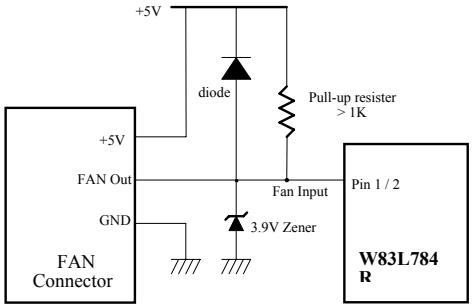


Figure 15-3. Fan with Tach Pull-Up to +5V and Zener Clamp

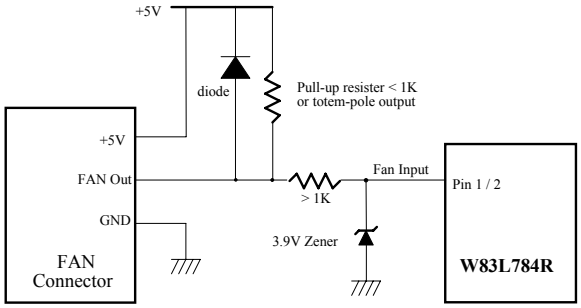


Figure 15-4. Fan with Tach Pull-Up to +5V, or Totem-Pole Putput and Zener Clamp

6.5.2 Fan speed control

The W83L784R/G provides four sets for fan PWM speed control. The duty cycle of PWM can be programmed by an 8-bit register which are defined in the Bank0 CR81h and CR83h. The default duty cycle is set to 100%, that is, the default 8-bit registers is set to FFh. The expression of duty can be represented as follows.

$$\text{Duty} - \text{cycle}(\%) = \frac{\text{Programmed 8 - bit Register Value}}{255} \times 100\%$$

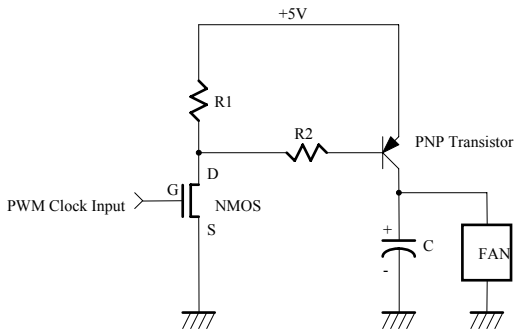


Figure 16

6.5.3 Smart Fan Control

Smart Fan Control provides two mechanisms. One is Thermal Cruise mode and the other is Fan Speed Cruise mode.

6.5.3.1. Thermal Cruise mode

At this mode, W83L784R/G provides the Smart Fan system which can control the fan speed automatically depend on current temperature to keep it with in a specific range. At first a wanted temperature and interval must be set (ex. 55 °C ± 3 °C) by BIOS, as long as the current temperature remains below the setting value, the fan will be off. Once the temperature exceeds the setting high limit temperature (58°C), the fan will be turned on with a specific speed set by BIOS (ex: 80% duty cycle) and automatically controlled its PWM duty cycle with the temperature varying. Three conditions may occur:

(1) If the temperature still exceeds the high limit (ex: 58°C), PWM duty cycle will increase slowly. If the fan has been operating in its fully speed but the temperature still exceeds the high limit (ex: 58°C), a warning message or a fan_fault signal(pin5) will be issued to protect the system.

(2) If the temperature goes below the high limit (ex: 58°C), but above the low limit (ex: 52°C), the fan speed will be fixed at the current speed because the temperature is in the target area (ex: 52 °C ~ 58°C).

(3) If the temperature goes below the low limit (ex: 52°C), PWM duty cycle will decrease slowly to 0 or a preset value until the temperature exceeds the low limit.

Figure 17 gives an illustration for Thermal Cruise Mode.

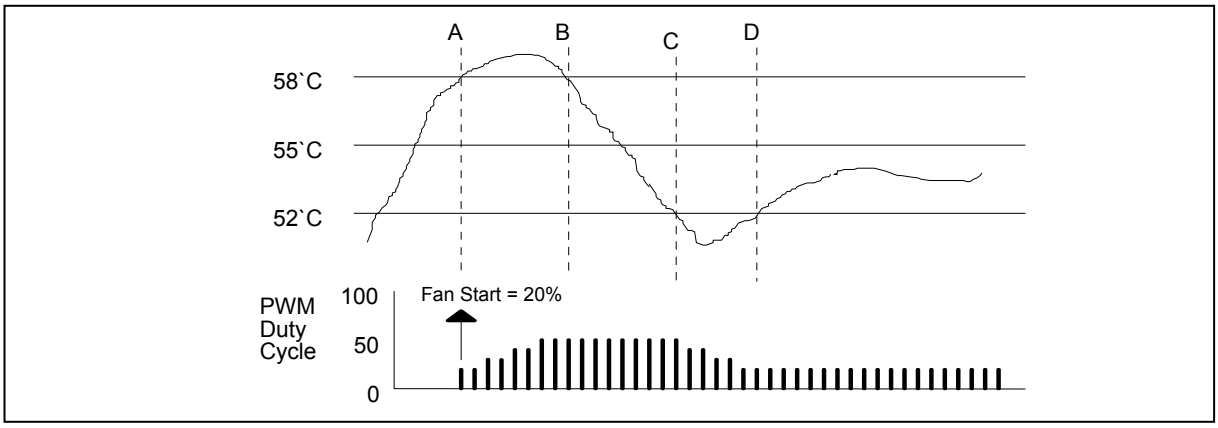


Figure 17-1

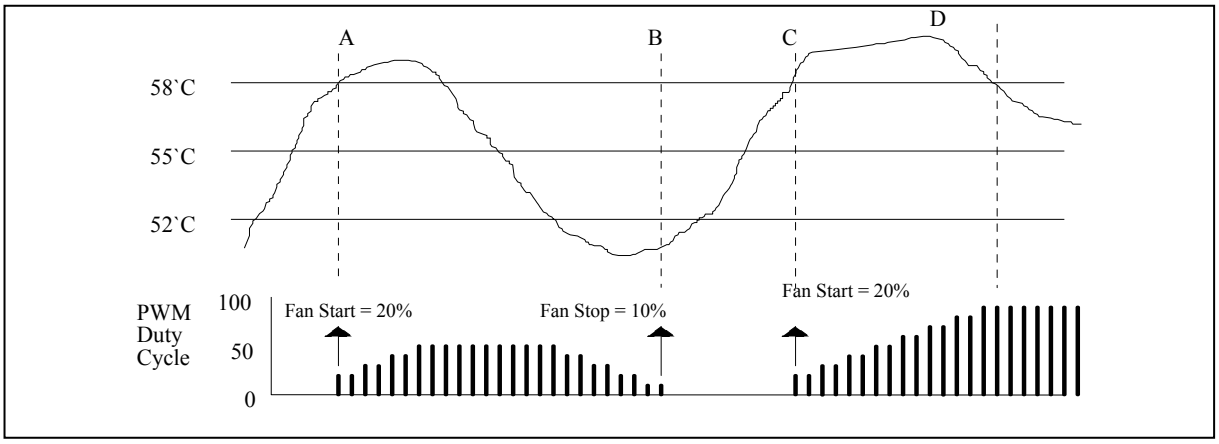


Figure 17-2

6.5.3.2. Fan Speed Cruise mode

At this mode, W83L784R/G provides the Smart Fan system which can control the fan speed automatically depend on current fan speed to keep it with in a specific range. A wanted fan speed count and interval must be set (ex. 160 ± 10) by BIOS. As long as the fan speed count is the specific range, PWM duty will keep the current value. If current fan speed count is higher than the high limit (ex. 160+10), PWM duty will be increased to keep the count less than the high limit. Otherwise, if current fan speed is less than the low limit (ex. 160-10), PWM duty will be decreased to keep the count higher than the low limit. See Figure 18 example.

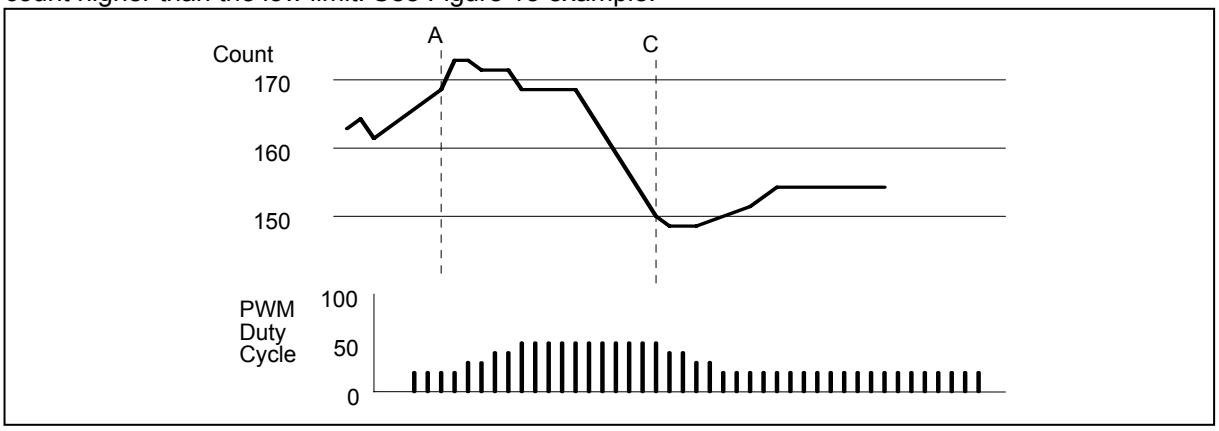


Figure 18

Of course, Smart Fan control system can be disabled and the fan speed control algorithm can be programmed by BIOS or application software.

6.5.4 Fan Fault Alarm

W83L784R/G can monitor fan speed by detecting fan speed counter value. When fan speed count is higher than high limit count value (CR58h) or less than low limit count value (CR59h), pin FANFAULT# is asserted.

6.6 SMI#

6.6.1 Temperature

Pin SMI# for temperature has 3 modes.

6.6.1.1. Comparator Interrupt Mode

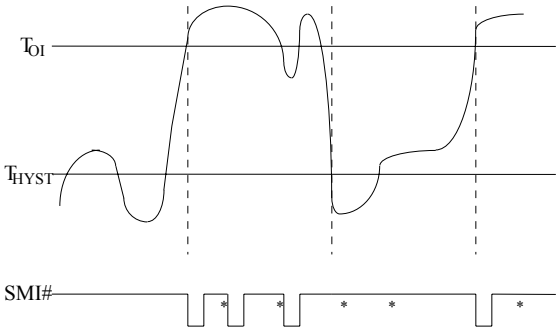
Temperature exceeding T_O causes an interrupt and this interrupt will be reset by reading all the Interrupt Status Registers. Once an interrupt event has occurred by exceeding T_O, then reset, if the temperature remains above the T_{HYST}, the interrupt will occur again when the next conversion has completed. If an interrupt event has occurred by exceeding T_O and not reset, the interrupts will not occur again. The interrupts will continue to occur in this manner until the temperature goes below T_{HYST}. (Figure 19-1)

6.6.1.2. Two-Times Interrupt Mode

Temperature exceeding T_O causes an interrupt and then temperature going below T_{HYST} will also cause an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. Once an interrupt event has occurred by exceeding T_O, then reset, if the temperature remains above the T_{HYST}, the interrupt will not occur. (Figure 19-2)

6.6.1.3. One-Time Interrupt Mode

Temperature exceeding T_O causes an interrupt and then temperature going below T_{HYST} will not cause an interrupt. Once an interrupt event has occurred by exceeding T_O, then going below T_{HYST}, an interrupt will not occur again until the temperature exceeding T_O. (Figure 19-3)



*Interrupt Reset when Interrupt Status Registers are read

Figure 19-1. Comparator Interrupt Mode

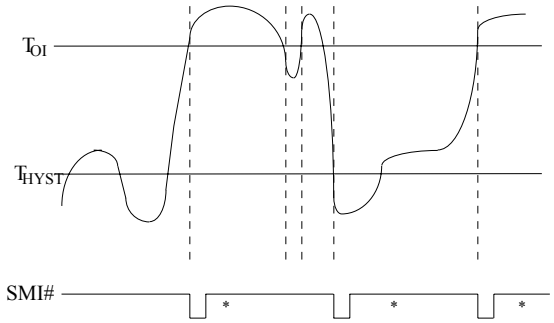
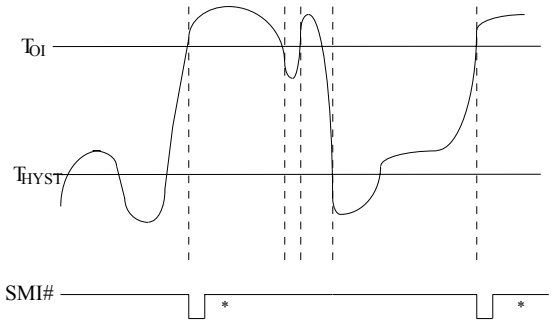


Figure 19-2. Two-Times Interrupt Mode



*Interrupt Reset when Interrupt Status Registers are read

Figure 19-3. One-Time Interrupt Mode

6.6.2 Voltage

SMI# interrupt for voltage is Two-Times Interrupt Mode. Voltage exceeding high limit or going below low limit will causes an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. (Figure 20-1)

6.6.3 Fan

SMI# interrupt for fan is Two-Times Interrupt Mode. Fan count exceeding the limit, or exceeding and then going below the limit (set at value ram index 3Bh and 3Ch) , will causes an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. (Figure 20-2)

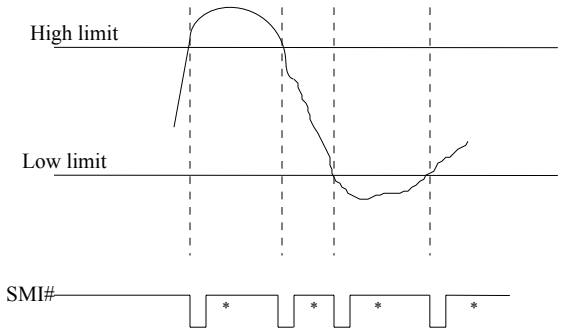


Figure 20-1. Voltage SMI# Mode

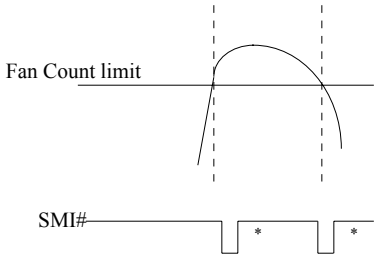


Figure 20-2. Fan SMI# Mode

*Interrupt Reset when Interrupt Status Registers are read

7. REGISTERS AND RAM

7.1 Configuration Register -- Index 40h

Power on default [7:0] = 0000, 0001 b

BIT	NAME	READ/WRITE	DESCRIPTION
7	INITIALIZATION	Read/Write	A one restores power on default value to all registers except the Serial Bus Address register. This bit clears itself since the power on default is zero.
6-4	Reserved	Read/Write	Reserved
3	DIS_PWROK	Read/Write	**Disable Power OK Function**. If this bit set to 1, the PWR_DN# (Pin 6) will keep logical high no mater what the pwoer VDD or +3.3V drop to the threshold voltage (4.0v and 2.6v, respectively).
2	Reserved	Reserved	Reserved
1	INT_ Clear	Read/Write	A one disables the SMI# outputs without affecting the contents of Interrupt Status Registers. The device will stop monitoring. It will resume upon clearing of this bit.
0	Start	Read/Write	A one enables startup of monitoring operation, a zero puts the part in standby mode. **Note:** The outputs of Interrupt pins will not be cleared if the user writes a zero to this location after an interrupt has occurred unlike "INT_Clear" bit.

7.2 Interrupt Status Register 1 -- Index 41h

Power on default [7:0] = 0000, 0000 b

BIT	NAME	READ/WRITE	DESCRIPTION
7	TEMP3	Read Only	A one indicates a High or Low limit has been exceeded from CPUT2 sensor.
6	TEMP2	Read Only	A one indicates a High or Low limit has been exceeded from CPUT1 sensor.
5	TEMP1	Read Only	A one indicates a High or Low limit has been exceeded from W83L784R internal temperature sensor.
4	Reserved	Reserved	Reserved
3	VCCIN	Read Only	A one indicates a High or Low limit has been exceeded. (VCC, +5V)
2	3VIN	Read Only	A one indicates a High or Low limit has been exceeded. (VIN2)
1	VBATIN	Read Only	A one indicates a High or Low limit has been exceeded.(VIN3)
0	VCOIN	Read Only	A one indicates a High or Low limit has been exceeded. (VIN1)

7.3 Interrupt Status Register 2 -- Index 42h

Power on default [7:0] = 0000, 0000 b

BIT	NAME	READ/WRITE	DESCRIPTION
7-4	Reserved	Read Only	Read 0.
3	TAR_T2	Read Only	**CPUT2 Target Status.** A one indicates CPUT2 temperature with Fan 2 full speed can not be in the specific range after 3 minutes.
2	TAR_T1	Read Only	**CPUT1 Target Status.** A one indicates CPUT1 temperature with Fan 1 full speed can not be in the specific range after 3 minutes.
1	FAN2	Read Only	A one indicates the fan count limit has been exceeded.
0	FAN1	Read Only	A one indicates the fan count limit has been exceeded.

7.4 SMI Mask Register 1 -- Index 43h

Power on default <7:0> = 0000, 0000 b

BIT	NAME	READ/WRITE	DESCRIPTION
7	MSK_T3_SMI	Read/Write	A one disables the corresponding interrupt status bit for $\overline{\text{SMI}}$ interrupt.(CPUT2 target temperature)
6	MSK_T2_SMI	Read/Write	A one disables the corresponding interrupt status bit for $\overline{\text{SMI}}$ interrupt.(CPUT1 target temperature)
5	MSK_T1_SMI	Read/Write	A one disables the corresponding interrupt status bit for $\overline{\text{SMI}}$ interrupt. (internal thermal diode)
4	Reserved	Reserved	Reserved
3	MSK_VCC_SMI	Read/Write	A one disables the corresponding interrupt status bit for $\overline{\text{SMI}}$ interrupt. (VCC, +5V)
2	MSK_3V_SMI	Read/Write	A one disables the corresponding interrupt status bit for $\overline{\text{SMI}}$ interrupt. (Pin VIN2)
1	MSK_VBAT_SMI	Read/Write	A one disables the corresponding interrupt status bit for $\overline{\text{SMI}}$ interrupt.(Pin VIN3)
0	MSK_VCO_SMI	Read/Write	A one disables the corresponding interrupt status bit for $\overline{\text{SMI}}$ interrupt. (Pin VIN1)

7.5 SMIÝ Mask Register 2 -- Index 44h

Power on default [7:0] = 0000, 0000 b

BIT	NAME	READ/WRITE	DESCRIPTION
7-4	Reserved	Read/Write	Reserved.
3	MSK_TAR2_SMI	Read/Write	A one disables the corresponding interrupt status bit for $\overline{SMI}$ interrupt. (CPUT2 target temperature)
2	MSK_TAR1_SMI	Read/Write	A one disables the corresponding interrupt status bit for $\overline{SMI}$ interrupt. (CPUT1 target temperature)
1	MSK_FAN2_SMI	Read/Write	A one disables the corresponding interrupt status bit for $\overline{SMI}$ interrupt. (Fan 2 speed counter)
0	MSK_FAN1_SMI	Read/Write	A one disables the corresponding interrupt status bit for $\overline{SMI}$ interrupt. (Fan 1 speed counter)

7.6 Real Time Hardware Status Register I -- Index 45h

Power on - [7:0] = 0000, 0000 b

BIT	NAME	READ/WRITE	DESCRIPTION
7	TEMP3_STS	Read Only	Temperature sensor 3 (CPU T2) Status. Set 1, the voltage of temperature sensor is over the limit value. Set 0, the voltage of temperature sensor is in the limit range.
6	TEMP2_STS	Read Only	Temperature sensor 2 (CPU T1) Status. Set 1, the voltage of temperature sensor is over the limit value. Set 0, the voltage of temperature sensor is in the limit range.
5	TEMP1_STS	Read Only	Temperature sensor 1 (Internal Thermal Diode) Status. Set 1, the voltage of temperature sensor is over the limit value. Set 0, the voltage of temperature sensor is in the limit range.
4	Reserved	Reserved	Reserved.
3	VCCIN_STS	Read Only	+5V Voltage Status. Set 1, the voltage of +5V is over the limit value. Set 0, the voltage of +5V is in the limit range.
2	3V_STS	Read Only	+3.3V Voltage Status. Set 1, the voltage of +3.3V is over the limit value. Set 0, the voltage of +3.3V is in the limit range.
1	VBAT_STS	Read Only	VBAT (VIN3) Voltage Status. Set 1, the voltage of VBAT (VIN3) is over the limit value. Set 0, the voltage of VBAT (VIN3) is in the limit range.
0	VCO_STS	Read Only	VCORE A Voltage Status. Set 1, the voltage of VCORE A is over the limit value. Set 0, the voltage of VCORE A is in the limit range.

7.7 Real Time Hardware Status Register II -- Index 46h

Power on default [7:0] = 0000-0000 b

Bit	Name	Read/Write	Description
7-4	Reserved	Read Only	Read 0.
3	TART2_STS	Read Only	**CPUT2 Target Status** Set 1, when CPUT2 target temperature with Fan 2 full speed can not be in the range after 3 minutes. Set 0, the temperature or speed is in the specific range.
2	TART1_STS	Read Only	**CPUT1 Target Status** Set 1, when CPUT1 target temperature with Fan 1 full speed can not be in the range after 3 minutes. Set 0, the temperature or speed is in the specific range.
1	FAN2_STS	Read Only	**FAN 2 Status** Set 1, the fan speed counter is over the limit value. Set 0, the fan speed counter is in the limit range.
0	FAN1_STS	Read Only	**FAN 1 Status** Set 1, the fan speed counter is over the limit value. Set 0, the fan speed counter is in the limit range.

7.8 Reserved Register -- Index 47h- 48h

Reserved

7.9 Fan Divisor Register -- Index 49h

Power on default [7:4] = 0001, 0001 b

BIT	NAME	READ/WRITE	DESCRIPTION
7	Reserved	Read/write	Reserved.
6-4	F2_SP_CRTL[2:0]	Read/Write	**FAN2 Speed Control.** 000 - divide by 1; 001 - divide by 2; 010 - divide by 4; 011 - divide by 8. 100 - divide by 16. 101 - divide by 32. 110 - divide by 64. 111 - divide by 128.
3	Reserved	Read/write	Reserved.
2-0	F1_SP_CTRL[2:0]	Read/Write	**FAN1 Speed Control.** 000 - divide by 1; 001 - divide by 2; 010 - divide by 4; 011 - divide by 8. 100 - divide by 16. 101 - divide by 32. 110 - divide by 64. 111 - divide by 128.

7.10 Serial Bus Address (for Voltage, Fan, and internal temperature) Register Address 4Ah

Power on default [7:0] = 0010, 1101 b

BIT	NAME	READ/WRITE	DESCRIPTION
7	Reserved	Read Only	
6-0	Serial Bus Address	Read/Write	Serial Bus address [6:0].

7.11 CPUT1 Temperature and CPUT2 Temperature Serial Bus Address Register Index 4Bh

Power on default [7:0] = 0000, 0001 b

BIT	NAME	READ/WRITE	DESCRIPTION
7	DIS_CPUT2	Read/Write	**Disable CPUT2 Temperature Function.** Set to 1, disable temperature 3 sensor and can not access any data from Temperature Sensor 3. Note that the relative functions of Status, and SMI# will be disable.
6-4	I2CADDR3[2:0]	Read/Write	**Temperature 3 Serial Bus Address.** The serial bus address is 1001xxx. Where xxx are defined in these bits.
3	DIS_CPUT1	Read/write	**Disable CPUT1 Temperature Function.** Set to 1, disable temperature Sensor and can not access any data from Temperature Sensor 2. Note that the relative functions of Status, and SMI# will be disable.
2-0	I2CADDR2[2:0]	Read/Write	**Temperature 2 Serial Bus Address.** The serial bus address is 1001xxx. Where xxx are defined in these bits.

7.12 Winbond Vendor ID (Low Byte) -- Index 4Ch (Auto Increase)

Power-on default [7:0] = 1010, 0011 b (A3h)

Bit	Name	Read/Write	Description
7:0	VIDL[7:0]	Read Only	Vendor ID Low Byte. Default A3h.

7.13 Winbond Vendor ID (High Byte) -- Index 4Dh (No Auto Increase)

Power-on default [7:0] = 0101, 1100 b (5Ch)

Bit	Name	Read/Write	Description
7:0	VIDH[7:0]	Read Only	**Vendor ID High Byte.** Default 5Ch

7.14 Chip ID -- Index 4Eh

Power on default [7:0] = 0101, 0000 b

BIT	NAME	READ/WRITE	DESCRIPTION
7-0	CHIPID[7:0]	Read Only	**Winbond Chip ID number.** Read this register will return 50h for W83L784R.

7.15 ACPI Temperature Increment Register -- Index 4Fh

Power on deafult [7:0] = 0000, 0101 b

BIT	NAME	READ/WRITE	DESCRIPTION
7	Reserved	Read/Write	Reserved.
6-0	DIFFREG[6:0]	Read/Write	**ACPI Temperature Increment Register.** If set to this register to non-zero value, the OVT# signal will be activated at pointer of the temperature of times of DIFFREG (i.e. DIFFREG*n, where n is non-zero integer). The default value is 5 degree C.

7.16 OVT# Property Select -- Index 50h

Power on default [7:0] = 0000, 0000 b

BIT	NAME	READ/WRITE	DESCRIPTION
7-6	Reserved	Read/Write	Reserved.
5-4	OVT_MD[1:0]	Read/Write	**OVT# Mode Select.** There are three OVT# signal output type. <00> - **Comparator Mode:** (Default) Temperature exceeding T_O causes the OVT# output activated until the temperature is less than T_{HYST}. <01> - **Interrupt Mode:** Setting temperature exceeding T_O causes the OVT# output activated indefinitely until reset reading temperature sensor 1/2/3 registers. Temperature exceeding T_O, then OVT# reset, and then temperature going below T_{HYST} will also cause the OVT# activated definitely until reset by reading temperature sensor 1/2/3. Once the OVT# will not be activated by exceeding T_O, and then reset, if the temperature remains above T_{HYST}, the OVT# will not be activated again. <10> - **ACPI Mode:** If set to 1 then enable ACPI OVT# output. Which is always send an OVT# signal when the temperature over the ACPI temperature increment value defined at Index 4Fh.

OVT# Property Select -- Index 50h, continued.

BIT	NAME	READ/WRITE	DESCRIPTION
3	EN_OVT3	Read/Write	Enable CPUT2 temperature sensor over-temperature (OVT) output if set to 1. Default 0, disable CPUT2 OVT output through pin OVT#. The pin OVT# is wire OR with OVT1 and OVT2.
2	EN_OVT2	Read/Write	Enable CPUT1 temperature sensor over-temperature (OVT) output if set to 1. Default 0, disable CPUT1 OVT output through pin OVT#. The pin OVT# is wire OR with OVT1 and OVT3.
1	EN_OVT1	Read/Write	Enable internal temperature sensor over-temperature (OVT) output if set to 1. Default 0, disable OVT1 output through pin OVT#. The pin OVT# is wire OR with OVT2 and OVT3.
0	OVTPOL	Read/Write	**Over-Temperature Polarity.** Write 1, OVT# active high. Write 0, OVT# active low. Default 0.

7.17 SMI# Property Select -- Index 51h

Power on - <7:0> --0000, 0100 b

BIT	NAME	READ/WRITE	DESCRIPTION
7-4	Reserved	Read/Write	Reserved.
3-2	TEMP_SMI_MD[1:0]	Read/Write	**Temperature SMI Mode Select.** <00> - **Comparator Interrupt Mode:** Temperature 1/2/3 exceeds T_O (Over-temperature) limit causes and interrupt and this interrupt will be reset by reading all the Interrupt Stauts. <01> - **Two Time Interrupt Mode:**(Default) This bit use in temperature sensor 1/2/3 interrupt mode with hysteresis type. Temperature exceeding T_O, causes an interrupt and then temperature going below T_{HYST} will also cause an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. Once an interrupt event has occurred by exceeding T_O, then reset, if the temperature remains above the T_{HYST}. <10> **- One Time Interrupt Mode:** This bit use in temperature sensor 1/2/3 interrupt mode with hysteresis type. Temperature exceeding T_O (Over-temperature, defined in Bank 1/2) causes an interrupt and then temperature going below T_{HYST} (Hysteresis temperature, defined in Bank 1/2) will not cause an interrupt. Once an interrupt event has occurred by exceeding T_O, then going below T_{HYST}, and interrupt will not occur again until the temperature exceeding T_O.

SMI# Property Select -- Index 51h, continued.

BIT	NAME	READ/WRITE	DESCRIPTION
1	EN_SMI#	Read/Write	**Enable SMI# Output.** A one enables the SMI# Interrupt output.
0	SMIPOL	Read/Write	**SMI# Polarity.** Write 1, SMI# active high. Write 0, SMI# active low. Default 0.

7.18 FANIN1/GPO1, FANIN2/GPO2 and BEEP/GPO3 Control Register -- Index 52h

Power on default [7:0] = 0000, 0000 b

BIT	NAME	READ/WRITE	DESCRIPTION
7	GPO4_VAL	Read/Write	**GPO4 Output Value.** GPO4 output value if EN_GPO4 is set to 1. Write 1, then pin 11 (GPO4) always generate logic high signal. Write 0, pin 11 (GPO4) always generates logic low signal. This bit default 0.
6	EN_GPO4	Read/Wite	**Enable GPO4 Function.** Set to 0 (default), pin 11 (BATFAULT#/GPO3) acts as BATFAULT# whcih is battery voltage out of the limit value. Set to 1, this pin 11 acts as GPO4 control function and the output value of GPO4 is programmed by this register bit 7.
5	GPO3_VAL	Read/Write	**GPO3 Output Value.** GPO3 output value if EN_GPO3 is set to 1. Write 1, then pin 5 (GPO3) always generate logic high signal. Write 0, pin 5 (GPO3) always generates logic low signal. This bit default 0.
4	EN_GPO3	Read/Wite	**Enable GPO3 Function.** Set to 0 (default), pin 5 (FANFAULT#/GPO3) acts as FAN_FAULT whcih is fan count out of the limit value. Set to 1, this pin 5 acts as GPO3 control function and the output value of GPO3 is programmed by this register bit 5.
3	GPO2_VAL	Read/Write	**GPO2 Output Value.** GPO2 output value if EN_GPO2 is set to 1. Write 1, then pin 2 (GPO2) always generate logic high signal. Write 0, pin 2 (GPO2) always generates logic low signal. This bit default 0.
2	EN_GPO2	Read/Write	**Enable GPO2 Function.** Which enable multiple function pin 2, named FANIN2/GPO2, GPO2 function. Set to 0 (default), pin 2 (FANIN2/GPO2) acts as FANIN2 whcih is fan clock input. Set to 1, this pin 2 acts as GPO2 control function and the output value of GPO2 is programmed by this register bit 3. This output pin GPO2 can connect to power PMOS gate to control FAN ON/OFF.
1	GPO1_VAL	Read/Write	**GPO1 Output Value.** GPO1 output value if EN_GPO1 is set to 1. Write 1, then pin 1 (GPO1) always generate logic high signal. Write 0, pin 1 (GPO1) always generates logic low signal. This bit default 0.

FANIN1/GPO1, FANIN2/GPO2 and BEEP/GPO3 Control Register -- Index 52h,,continued.

BIT	NAME	READ/WRITE	DESCRIPTION
0	EN_GPO1	Read/Write	**Enable GPO1 Function.** Which enable multiple function pin 1, named FANIN1/GPO1, GPO1 function. Set to 0 (default), pin 1 (FANIN1/GPO1) acts as FANIN1 whcih is fan clock input. Set to 1, this pin 1 acts as GPO1 control function and the output value of GPO1 is programmed by this register bit 1. This output pin GPO2 can connect to power PMOS gate to control FAN ON/OFF.

7.19 CPUT1/CPUT2 Thermal Sensor Type Register -- Index 53h

Power on default [7:0] = 0000-0000 b

BIT	NAME	READ/WRITE	DESCRIPTION
7-4	Reserved	Read/Write	Reserved.
3-2	T3_TYPE[1:0]	Read/Write	Temperature sensor 3 (CPU T2) type. 0x - Thermistor (10K @ 25 degree C, B=3435). 10 - 2N3904 transistor. 11 - Intel thermal diode.
1-0	T2_TYPE[1:0]	Read/Write	Temperature sensor 2 (CPU T1) type. 0x - Thermistor (10K @ 25 degree C, B=3435) 10 - 2N3904 transistor 11 - Intel thermal diode.

7.20 Misc Control Register -- Index 54h

Power on default [7:0] = 0000-0000 b

BIT	NAME	READ/WRITE	DESCRIPTION
7-6	Reserved	Read/Write	Reserved.
5	PWM2_LM_Enable	Read/Write	Set 1, PWMOUT2 duty cycle will decrease to CR [89h] when temperature goes below target range. Set 0, PWMOUT2 duty cycle will decrease to 0 when temperature grows below target range.
4	PWM1_LM_Enable	Read/Write	Set 1, PWMOUT1 duty cycle will decrease to CR [88h] when temperature goes below target range. Set 0, PWMOUT1 duty cycle will decrease to 0 when temperature grows below target range.
3	Reserved	Reserved	Reserved
2	SWP_FAN2_PWM	Read/Write	**Swap CPUT2 PWM to internal temperature sensor PWM Control.** Write this bit set to 1, FAN2 PWM PWM control will refer to internal temperature sensor.

Misc Control Register -- Index 54h, continued.

BIT	NAME	READ/WRITE	DESCRIPTION
1	Reserved	Reserved	Reserved
0	EN_VBAT_MNT	ReadWrite	Write 1, enable battery voltage monitor. Write 0, disable battery voltage monitor. (VIN4/VBAT)

7.21 Fan/VBAT Fault Control Register -- Index 55h

Power on default [7:0] = 0000-0000 b

BIT	NAME	READ/WRITE	DESCRIPTION
7-3	Reserved	Read/Write	Reserved.
2	EN_FAN2_FAULT	Read/Write	**Enable Fan 2 Fault Function.** When Fan 2 is out of the Fan Fault Limit value (defined Index 58 and 59), the Pin 5 will go to low level. This function is wire-or with Fan 1 fault if fan 1 fualt function is enable.
1	EN_FAN1_FAULT	Read/Write	**Enable Fan1 Fault Function.** When Fan 1 is out of the Fan Fault Limit value (defined Index 56 and 57), the Pin 5 will go to low level. This function is wire-or with Fan 2 fault if fan 2 fualt function is enable.
0	EN_VBAT_FAULT	Read/Write	**Enable VBAT Fault Function**. Set to 1, enable battery fault function. Set to 0, disable this function. When battery voltage is out of the fault limit value (defined at Index 5A and 5B), the Pin 11 (BATFAULT#) will be asserted.

7.22 Fan 1 Fault High Limit Count -- Index 56h

Power on default [7:0] = 1111-1111 b

BIT	NAME	READ/WRITE	DESCRIPTION
7-0	FAN_HI_LM	Read/Write	**Fan High Count Limit Value.**

7.23 Fan 2 Fault Low Limit Count -- Index 57h

Power on default [7:0] = 0000-0000 b

BIT	NAME	READ/WRITE	DESCRIPTION
7-0	FAN_LOW_LM	Read/Write	**Fan Low Count Limit Value.**

7.24 Fan 2 Fault High Limit Count -- Index 58h

Power on default [7:0] = 1111-1111 b

Bit	Name	Read/Write	Description
7-0	FAN_HI_LM	Read/Write	**Fan High Count Limit Value.**

7.25 Fan 1 Fault Low Limit Count -- Index 59h

Power on default [7:0] = 0000-0000 b

Bit	Name	Read/Write	Description
7-0	FAN_LOW_LM	Read/Write	**Fan Low Count Limit Value.**

7.26 VBAT Fault High Limit Value -- Index 5Ah

Power on default [7:0] = 1111-1111 b

BIT	NAME	READ/WRITE	DESCRIPTION
7-0	VBAT_HI_LM	Read/Write	**VBAT High Limit Value.**

7.27 VBAT Fault Low Limit Value -- Index 5Bh

Power on default [7:0] = 0000-0000 b

Bit	Name	Read/Write	Description
7-0	VBAT_LOW_LM	Read/Write	**VBAT Low Limit Value.**

7.28 FAN 1 Pre-Scale Register -- Index 80h

Power on default [7:0] = 0000-0001 b

BIT	NAME	READ/WRITE	DESCRIPTION
7	PWM_CLK_SEL1	Read/Write	**PWM Input Clock Select.** This bit select Fan 1 input clock to pre-scale divider. 0: 1 MHz 1: 125 KHz
6-0	PRE_SCALE1[6:0]	Read/Write	**Fan 1 Input Clock Pre-Scale.** The divider of input clock is the number defined by pre-scale. Thus, writing 0 transfers the input clock directly to counter. The maximum divider is 128 (7Fh). 00h : divider is 1 01h : divider is 2 02h : divider is 3 : :

7.29 FAN 1 Duty Cycle Select Register -- 81h (Bank 0)

Power on default [7:0] 1111, 1111 b

BIT	NAME	READ/WRITE	DESCRIPTION
7-0	F1_DC[7:0]	Read/Write	**Fan 1 Duty Cycle.** This 8-bit register determines the number of input clock cycles, out of 256-cycle period, during which the PWM output is high. During smart fan 1 control mode, read this register will return smart fan duty cycle. 00h: PWM output is always logical Low. FFh: PWM output is always logical High. XXh: PWM output logical High percentage is (XX/256*100%) during one cycle.

7.30 FAN 2 Pre-Scale Register -- Index 82h

Power on default [7:0] = 0000, 0001 b

BIT	NAME	READ/WRITE	DESCRIPTION
7	PWM_CLK_SEL2	Read/Write	**PWM 2 Input Clock Select.** This bit select Fan 2 input clock to pre-scale divider. 0: 1 MHz 1: 125 KHz
6-0	PRE_SCALE2[6:0]	Read/Write	**Fan 2 Input Clock Pre-Scale.** The divider of input clock is the number defined by pre-scale. Thus, writing 0 transfers the input clock directly to counter. The maximum divider is 128 (7Fh). 00h : divider is 1 01h : divider is 2 02h : divider is 3 : :

7.31 FAN2 Duty Cycle Select Register -- Index 83h

Power on default [7:0] = 1111, 1111 b

BIT	NAME	READ/WRITE	DESCRIPTION
7-0	F2_DC[7:0]	Read/Write	**Fan 2 Duty Cycle.** This 8-bit register determines the number of input clock cycles, out of 256-cycle period, during which the PWM output is high. During smart fan 2 control mode, read this register will return smart fan duty cycle. 00h: PWM output is always logical Low. FFh: PWM output is always logical High. XXh: PWM output logical High percentage is XX/256*100% during one cycle.

7.32 FAN Configuration Register -- Index 84h

Power on default [7:0] = 0000, 0000 b

BIT	NAME	READ/WRITE	DESCRIPTION
7-2	Reserved	Read/Write	Reserved
5-4	FAN2_MODE	Read/Write	FAN 2 PWM Control Mode. 00 - Manual PWM Control Mode. (Default) 01 - Thermal Cruise mode. 10 - Fan Speed Cruise Mode. 11 - Reserved.
3-2	FAN1_MODE	Read/Write	FAN 1 PWM Control Mode. 00 - Manual PWM Control Mode. (Default) 01 - Thermal Cruise mode. 10 - Fan Speed Cruise Mode. 11 - Reserved.
1	FAN2_OB	Read/Write	**Enable Fan 2 as Output Buffer.** Set to 1, FANPWM1 can drive logical high or logical low. Default Pin 4 (FANPWM) is open-drain.
0	FAN1_OB	Read/Write	**Enable Fan 1 as Output Buffer.** Set to 1, FANPWM1 can drive logical high or logical low. Default Pin 3 (FANPWM) is open-drain.

7.33 CPUT1 Target Temperature Register/ Fan 1 Target Speed Register -- Index 85h

Power on default [7:0] = 0000, 0000 b

CPUT1 target temperature register for Thermal Cruise mode.

BIT	NAME	READ/WRITE	DESCRIPTION
7	Reserved	Read/Write	**Reserved.**
6-0	TEMP_TAR_T1[6:0]	Read/Write	**CPUT1 Target Temperature.** Only for Thermal Cruise Mode while CR84h bit3-2 is 01.

Fan 1 target speed register for Fan Speed Cruise mode.

BIT	NAME	READ/WRITE	DESCRIPTION
7-0	SPD_TAR_FAN1 [7:0]	Read/Write	**Fan 1 Target Speed Control.** Only for Fan Speed Cruise Mode while CR84h bit3-2 is 10.

7.34 CPUT2 Target Temperature Register/ Fan 2 Target Speed Register -- Index 86h

Power on - [7:0] = 0000, 0000 b

CPUT2 target temperature register for Thermal Cruise mode.

BIT	NAME	READ/WRITE	DESCRIPTION
7	Reserved	Read/Write	**Reserved.**
6-0	TEMP_TAR_T2[6:0]	Read/Write	**CPUT1 Target Temperature.** Only for Thermal Cruise Mode while CR84h bit5-4 is 01.

Fan 2 target speed register for Fan Speed Cruise mode.

BIT	NAME	READ/WRITE	DESCRIPTION
7-0	SPD_TAR_FAN 2[7:0]	Read/Write	**Fan 1 Target Speed Control.** Only for Fan Speed Cruise Mode while CR84h bit5-4 is 10.

7.35 Tolerance of Target Temperature or Target Speed Register -- Index 87h

Power on default [7:0] = 0001, 0001 b

Tolerance of CPUT1/CPUT2 target temperature register.

BIT	NAME	READ/WRITE	DESCRIPTION
7-4	TOL_T2[3:0]	Read/Write	**Tolerance of Fan 2 Target Temperature.** Only for Thermal Cruise mode.
3-0	TOL_T1[3:0]	Read/Write	**Tolerance of Fan 1 Target Temperature.** Only for Thermal Cruise mode.

Tolerance of Fan 1/2 target speed register.

BIT	NAME	READ/WRITE	DESCRIPTION
7-4	TOL_FS2[3:0]	Read/Write	**Tolerance of Fan 2 Target Speed Count.** Only for Fan Speed Cruise mode.
3-0	TOL_FS1[3:0]	Read/Write	**Tolerance of Fan 1 Target Speed Count.** Only for Fan Speed Cruise mode.

7.36 Fan 1 PWM Stop Duty Cycle Register -- Index 88h

Power on default [7:0] = 0000, 0001 b

BIT	NAME	READ/WRITE	DESCRIPTION
7-0	STOP_DC1[7:0]	Read/Write	In Thermal Cruise mode, PWM duty will be 0 if it decreases to under this value. This register should be written a non-zero minimum PWM stop duty cycle.

7.37 Fan 2 PWM Stop Duty Cycle Register -- 89h (Bank 0)

Power on default [7:0] = 0000, 0001 b

BIT	NAME	READ/WRITE	DESCRIPTION
7-0	STOP_DC2[7:0]	Read/Write	In Thermal Cruise mode, PWM duty will be 0 if it decreases to under this register value. This register should be written a non-zero minimum PWM stop duty cycle.

7.38 Fan 1 Start-up Duty Cycle Register -- Index 8Ah

Power on default [7:0] = 0000, 0001 b

BIT	NAME	READ/WRITE	DESCRIPTION
7-0	START_DC1[7:0]	Read/Write	In Thermal Cruise mode, PWM duty will increase from 0 to this register value to provide a minimum duty cycle to turn on the fan. This register should be written a fan start-up duty cycle.

7.39 Fan 2 Start-up Duty Cycle Register -- Index 8Bh

Power on default [7:0] = 0000, 0001 b

BIT	NAME	READ/WRITE	DESCRIPTION
7-0	START_DC2[7:0]	Read/Write	In Thermal Cruise mode, PWM duty will increase from 0 to this register value to provide a minimum duty cycle to turn on the fan. This register should be written a fan start-up duty cycle.

7.40 Fan 1 Stop Time Register -- Index 8Ch

Power on default [7:0] = 0011, 1100 b

BIT	NAME	READ/WRITE	DESCRIPTION
7-0	STOP_TIME1[7:0]	Read/Write	In Thermal Cruise mode, this register determines the time of which PWM duty is from stop duty cycle to 0 duty cycle. The unit of this register is 0.1 second. The default value is 6 seconds.

7.41 Fan 2 Stop Time Register -- Index 8Dh

Power on default [7:0] = 0011, 1100 b

BIT	NAME	READ/WRITE	DESCRIPTION
7-0	STOP_TIME2[7:0]	Read/Write	In Thermal Cruise mode, this register determines the time of which PWM duty is from stop duty cycle to 0 duty cycle. The unit of this register is 0.1 second. The default value is 6 seconds.

7.42 Fan Step down Time Register -- Index 8Eh

Power on default [7:0] = 0000, 1010 b

BIT	NAME	READ/WRITE	DESCRIPTION
7-0	STEP_UP_T[7:0]	Read/Write	The time interval, which is 0.1 second unit, to decrease PWM duty in Smart Fan Control mode.

7.43 Fan Step up Time Register -- Index 8Fh

Power on default [7:0] = 0000, 1010 b

BIT	NAME	READ/WRITE	DESCRIPTION
7-0	STEP_DOWN_T [7:0]	Read/Write	The time interval, which is 0.1 second unit, to increase PWM duty in Smart Fan Control mode.

7.44 Temperature Sensor 1 (Internal Thermal Diode) Offset Register -- Index 90h

Power-on default [7:0] = 0000, 0000 b

BIT	NAME	READ/WRITE	DESCRIPTION
7-6	Reserved	Read/Write	Reserved.
5-0	OFFSET1[5:0]	Read/Write	Temperature 1 base temperature. This value is added to monitor value, resulting in the current temperature. 01,1111 => +31 degree C 01,1110 => +30 degree C : 00,0001 => +1 degree C 00,0000 => +0 degree C 11,1111 => -1 degree C 11,1110 => -2 degree C : 10,0000 => -32 degree

7.45 Temperature Sensor 2 (CPU T1) Offset Register -- Index 91h

Power-on default [7:0] = 0000, 0000 b

BIT	NAME	READ/WRITE	DESCRIPTION
7-6	Reserved	Read/Write	Reserved.
5-0	OFFSET1[5:0]	Read/Write	Temperature 2 (CPUT1) base temperature. This value is added to monitor value, resulting in the current temperature. 01,1111 => +31 degree C 01,1110 => +30 degree C : 00,0001 => +1 degree C 00,0000 => +0 degree C 11,1111 => -1 degree C 11,1110 => -2 degree C : 10,0000 => -32 degree

7.46 Temperature Sensor 3 (CPU T2) Offset Register -- Index 92h

Power-on default [7:0] = 0000, 0000 b

BIT	NAME	READ/WRITE	DESCRIPTION
7-6	Reserved	Read/Write	Reserved.
5-0	OFFSET3[5:0]	Read/Write	Temperature 3 (CPU T2) base temperature. This value is added to monitor value, resulting in the current temperature. 01,1111 => +31 degree C 01,1110 => +30 degree C : 00,0001 => +1 degree C 00,0000 => +0 degree C 11,1111 => -1 degree C 11,1110 => -2 degree C : 10,0000 => -32 degree

8. VALUE RAM AND LIMIT VALUE

8.1 Value RAM -- Index 20h- 3Fh or 60h - 7Fh

INDEX A6-A0	INDEX A6-A0	DESCRIPTION
20h	60h	Pin VIN1 reading (Vcore)
21h	61h	Pin VIN3 reading (VBAT)
22h	62h	Pin VIN2 reading (+3.3V)
23h	63h	Pin VCC reading (VCC,+5V)
24h	64h	Reserved
25h	65h	Reserved
26h	66h	Reserved
27h	67h	Internal Temperature reading
28h	68h	FAN1 reading **Note:** This location stores the number of counts of the internal clock per revolution.
29h	69h	FAN2 reading **Note:** This location stores the number of counts of the internal clock per revolution.
2Ah	6Ah	Reserved
2Bh	6Bh	VIN1(Vcore) High Limit
2Ch	6Ch	VIN1(Vcore) Low Limit
2Dh	6Dh	VIN3 (VBAT) High Limit
2Eh	6Eh	VIN3 (VBAT) Low Limit
2Fh	6Fh	VIN2 (+3.3V) High Limit
30h	70h	VIN2 (+3.3V) Low Limit
31h	71h	VCC High Limit
32h	72h	VCC Low Limit
33h	73h	Reserved
34h	74h	Reserved
35h	75h	Reserved
36h	76h	Reserved
37h	77h	Reserved
38h	78h	Reserved
39h	79h	Over Temperature Limit (High) of internal temperature
3Ah	7Ah	Temperature Hysteresis Limit (Low) of internal temperature
3Bh	7Bh	FAN1 Fan Count Limit
3Ch	7Ch	FAN2 Fan Count Limit.
3Dh	7Dh	Reserved
3E- 3Fh	7E- 7Fh	Reserved

9. TEMPERATURE SENSOR 2 (CPU T1) REGISTERS

The address of I^2C is defined in Bank0.Reg4B.

9.1 Temperature Sensor 2 Temperature Register -- Index 00h

Read Only

BIT	NAME	READ/WRITE	DESCRIPTION
15-7	TEMP2[8:0]	Read Only	Temperature bit [8:0] of sensor 2. (0.5 degree C precision)
6-0	Reserved	Read Only	Read 0.

9.2 Temperature Sensor 2 Configuration Register -- Index 01h

Power-on default [7:0] = 0000, 0000 b

BIT	NAME	READ/WRITE	DESCRIPTION
7-5	Reserved	Read	Read 0.
4-3	FAULT	Read/Write	Number of faults to detect before setting OVT# output to avoid false tripping due to noise.
2-1	Reserved	Read/Write	Reserved.
0	Reserved	Read/Write	Reserved.

9.3 Temperature Sensor 2 Hysteresis Register -- Index 02h

Power-on - <15:0> = 0100,1011,0000,0000 b

BIT	NAME	READ/WRITE	DESCRIPTION
15-7	THYST2[8:0]	Read/Write	Temperature hysteresis bit 8-0. The temperature default 75.0 degree C.
6:0	Reserved	Read	Read 0.

9.4 Temperature Sensor 2 Over-temperature Register -- Index 03h

Power-on - <15:0> = 0101,0000,0000,0000 b

BIT	NAME	READ/WRITE	DESCRIPTION
15-7	TOVF2[8:0]	Read/Write	Over-temperature bit 8-0. The temperature default 80.0 degree C.
6:0	Reserved	Read	Read 0.

10. TEMPERATURE SENSOR 3 (CPU T2) REGISTERS

The address of I^2C is defined in Bank0.Reg4B.

10.1 Temperature Sensor 3 Temperature Register -- Index 00h

Read Only

BIT	NAME	READ/WRITE	DESCRIPTION
15-7	TEMP2[8:0]	Read Only	Temperature bit [8:0] of sensor 2. (0.5 degree C precision).
6-0	Reserved	Read Only	Read 0.

10.2 Temperature Sensor 3 Configuration Register -- Index 01h

Power-on - [7:0] = 0000, 0000 b

BIT	NAME	READ/WRITE	DESCRIPTION
7-5	Reserved	Read	Read 0.
4-3	FAULT	Read/Write	Number of faults to detect before setting OVT# output to avoid false tripping due to noise.
2-1	Reserved	Read Only	Read 0.
0	Reserved	Read/Write	Reserved

10.3 Temperature Sensor 3 Hysteresis Register -- Index 02h

Power-on default [15:0] = 0100,1011,0000,0000 b

BIT	NAME	READ/WRITE	DESCRIPTION
15-7	THYST3[8:0]	Read/Write	Temperature hysteresis bit 8-0. The temperature default 75.0 degree C.
6-0	Reserved	Read Only	Read 0.

10.4 Temperature Sensor 3 Over-temperature Register -- Index 03h

Power-on - [15:0] = 0101,0000,0000,0000 b

BIT	NAME	READ/WRITE	DESCRIPTION
15-7	TOVF3[8:0]	Read/Write	Over-temperature bit 8-0. The temperature default 80.0 degree C.
6-0	Reserved	Read Only	Read 0.

11. SPECIFICATIONS

11.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage	-0.5 to 7.0	V
Input Voltage	-0.5 to V_{DD}+0.5	V
Operating Temperature	0 to +70	° C
Storage Temperature	-55 to +150	° C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

11.2 DC Characteristics

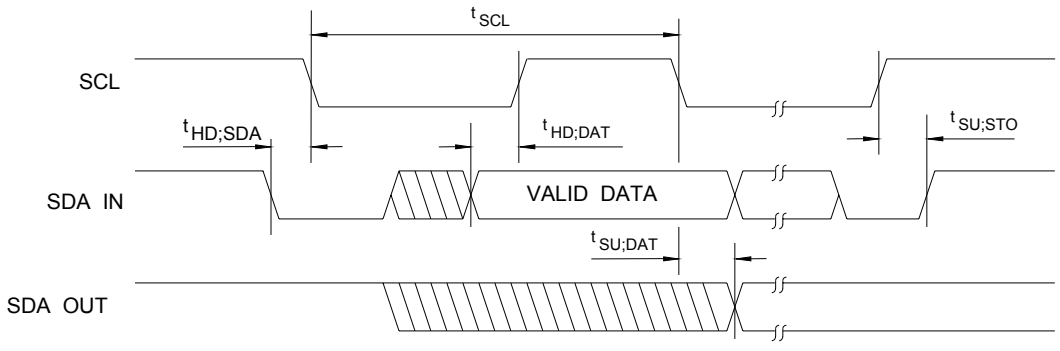
(Ta = 0° C to 70° C, V_{DD} = 5V ± 10%, V_{SS} = 0V)

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I/O_{12t} - TTL level bi-directional pin with source-sink capability of 12 mA						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = - 12 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = V_{DD}
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V
I/O_{12ts} - TTL level bi-directional pin with source-sink capability of 12 mA and schmitt-trigger level input						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{DD} = 5 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{DD} = 5 V
Hysteresis	V_{TH}	0.5	1.2		V	V_{DD} = 5 V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = - 12 mA
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = V_{DD}
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0V
OUT_{12t} - TTL level output pin with source-sink capability of 12 mA						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
OD_8 - Open-drain output pin with sink capability of 8 mA						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA

DC Characteristics, continued.

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
OD_{12} - Open-drain output pin with sink capability of 12 mA						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
OD_{48} - Open-drain output pin with sink capability of 48 mA						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 48 mA
IN_t - TTL level input pin						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = V_{DD}
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V
IN_{ts} - TTL level Schmitt-triggered input pin						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{DD} = 5 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{DD} = 5 V
Hysteresis	V_{TH}	0.5	1.2		V	V_{DD} = 5 V
Input High Leakage	I_{LIH}			+10	μA	V_{IN} = V_{DD}
Input Low Leakage	I_{LIL}			-10	μA	V_{IN} = 0 V

11.3 AC Characteristics



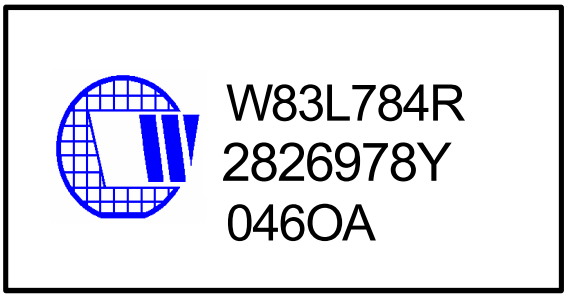
Serial Bus Timing Diagram

Serial Bus Timing

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
SCL clock period	t_{SCL}	10		uS
Start condition hold time	$t_{HD;SDA}$	4.7		uS
Stop condition setup-up time	$t_{SU;STO}$	4.7		uS
DATA to SCL setup time	$t_{SU;DAT}$	120		nS
DATA to SCL hold time	$t_{HD;DAT}$	5		nS
SCL and SDA rise time	t_R		1.0	uS
SCL and SDA fall time	t_F		300	nS

12. HOW TO READ THE TOP MARKING

The top marking of W83L784R



Left: Winbond logo

1st line: Winbond logo and the type number: W83L784R

2nd line: Tracking code 2 826978Y

2: wafers manufactured in Winbond FAB 2

826978Y: wafer production series lot number

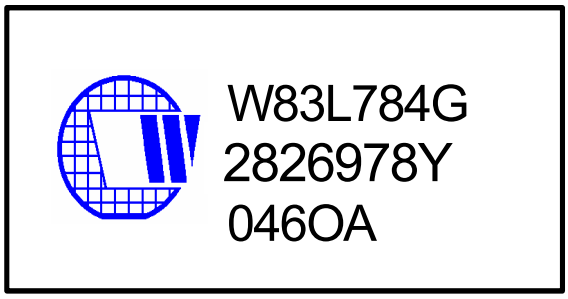
3rd line: Tracking code 046 O B

046: packages made in '00, week 46

O: assembly house ID; A means ASE, S means SPIL, O means OSE

A: IC revision

The top marking of W83L784G



Left: Winbond logo

1st line: Winbond logo and the type number: W83L784G

2nd line: Tracking code 2 826978Y

2: wafers manufactured in Winbond FAB 2

826978Y: wafer production series lot number

3rd line: Tracking code 046 O B

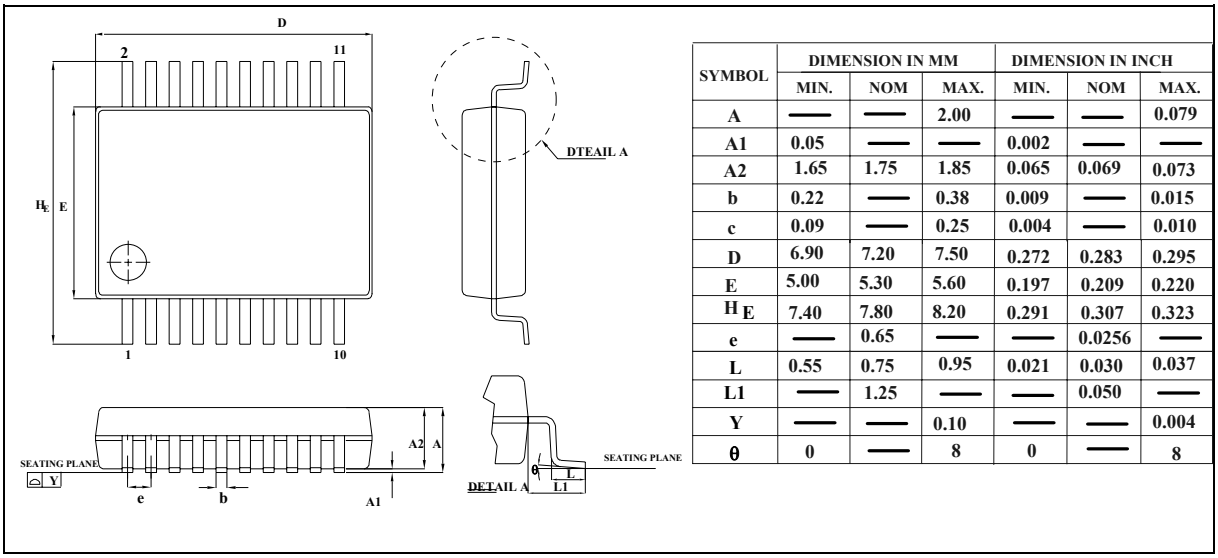
046: packages made in '00, week 46

O: assembly house ID; A means ASE, S means SPIL, O means OSE

A: IC revision

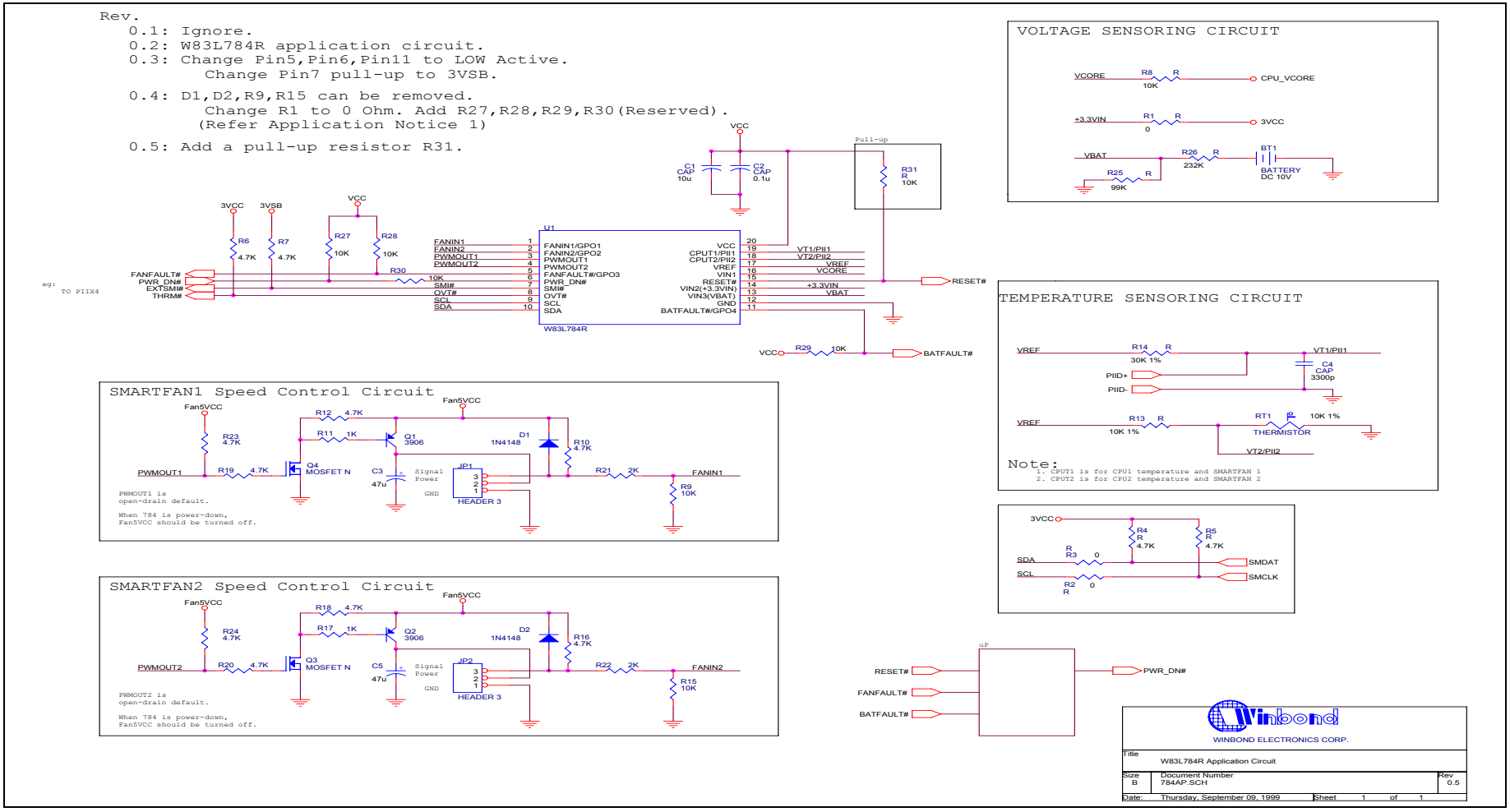
13. PACKAGE DRAWING AND DIMENSIONS

20 SSOP-209 mil



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	—	—	2.00	—	—	0.079
A1	0.05	—	—	0.002	—	—
A2	1.65	1.75	1.85	0.065	0.069	0.073
b	0.22	—	0.38	0.009	—	0.015
c	0.09	—	0.25	0.004	—	0.010
D	6.90	7.20	7.50	0.272	0.283	0.295
E	5.00	5.30	5.60	0.197	0.209	0.220
HE	7.40	7.80	8.20	0.291	0.307	0.323
e	—	0.65	—	—	0.0256	—
L	0.55	0.75	0.95	0.021	0.030	0.037
L1	—	1.25	—	—	0.050	—
Y	—	—	0.10	—	—	0.004
θ	0	—	8	0	—	8

14. W83L784R/G SCHEMATICS



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